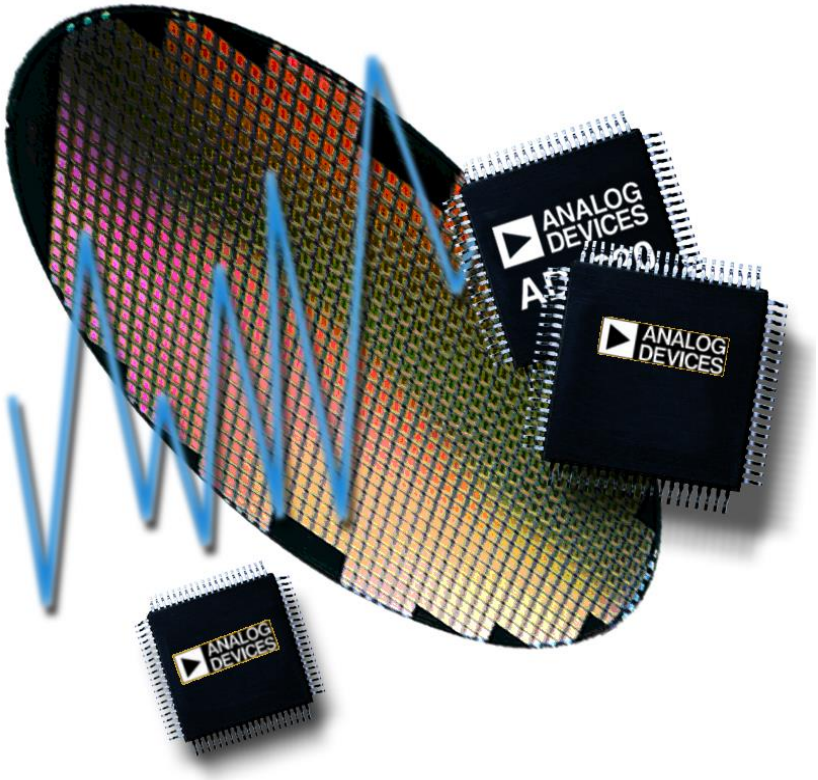


Reliability Report

Report Title: ADSP-21479W-02 Automotive Grade 2 at UT2 Qualification

Report Number: 17607

Revision: A

Date: 27 July 2022

Summary

This report documents the successful completion of the reliability qualification requirements for the release of the ADSP-21479W-02 automotive grade 2 product in an 88-LFCSP package at UTAC (UT2). The ADSP-21479W-02 SHARC® processor is a member of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. Table 1 describes the ADSP-21479W-02 product characteristics.

Table 1: ADSP-21479W-02 Product Characteristics

Die/Fab

Die Id	TMAP60 D-T2
Die Size (mm)	4.74 x 5.44
Wafer Fabrication Site	E_TSMC1212
Wafer Fabrication Process	65nm CMOS
Approximate Transistor Count	50.0 million
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu(0.5%)
Polyimide	Yes

Package/Assembly

Package	88-LFCSP
Body Size (mm)	12.00 x 12.00 x 0.85
Assembly Location	UTAC (UT2)
Molding Compound	Sumitomo G700LTD
Die Attach	Ablestik 8600 conductive
Wire Type	4N Gold
Wire Diameter (mil)	1.00
Lead Frame Material	Copper
Lead Finish	NA
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Table 2 provides a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: LFCSP at UTAC (UT2) Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Highly Accelerated Temperature and Humidity Stress Test (HAST)[1,2]	JESD22-A110	130C 85%RH 33.3 psia, Biased, 192 Hours	LT8355-1	Q19285.1ABHAST	77	0
			LT8277	Q19306.1BHAST	77	0
				Q19306.2HAST	77	0
			LT8390	Q19204.2BHAST	77	0
			LT8391D	Q19204.3BHAST	77	0
		130C 85%RH 33.3 psia, Biased, 96 Hours	MAX25500ATMA/V+	R41514A	77	0
				R41514B	77	0
				R41514C	77	0
			MAX20081ATNK/V+	R41199A	77	0
				R41199B	77	0
				R41199C	77	0
			MAX20069BGTLA/VY+	JCFZ1A012BQ	77	0
				JCFZ1A012BA	77	0
				JCFZ1A012B	77	0
			MAX20028ATJA/VY+	JCTJ1Q002RC	77	0
				JCTJ1Q002RD	77	0
				JCTJ1Q002RE	77	0
			MAX20430ATIA/VY+	JCDD33003D	77	0
				JCDD33003G	77	0
				JCDD33003E	77	0
High Temperature Storage Life (HTSL)[2]	JESD22-A103	150°C, 1,000 Hours	ADSP-21479W-02	Q17607.1.HS1	77	0
Solder Heat Resistance (SHR) [1,3]	J-STD-020	MSL-3	ADSP-21479W-02	Q17607.1.SH1	11	0
				Q17607.2.SH2	11	0
				Q17607.3.SH3	11	0
Solderability	JESD22-B102	Soldering Temp of 245°C, Single Duration	ADSP-21479W-02	Q17607.1.ST1	15	0
Temperature Cycling (TC) [1,4,5]	JESD22-A104	-55°C/+125°C, 1,000 Cycles	ADSP-21479W-02	Q17607.1.TC1	77	0
				Q17607.2.TC2	77	0
				Q17607.3.TC3	77	0
Unbiased HAST (UHST) [1,3]	JESD22-A118	130C 85%RH 33.3 psia, 96 Hours	ADSP-21479W-02	Q17607.1.UH1	77	0
				Q17607.2.UH2	77	0
				Q17607.3.UH3	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

[2] Electrical test was performed at room and hot temperatures.

[3] Electrical test was performed at room temperature.

[4] Electrical test was performed at hot temperature.

[5] Post-TCT wire bond pull testing was performed per AEC-Q100 on five units each from TCT lots Q17607.1.TC1, Q17607.2.TC2 and Q17607.3.TC3. Minimum bond pull results were 8.270 grams, 8.843 grams and 9.190 grams respectively. Complete data for the five units each lot are presented in Appendix A of this report.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Field-Induced Charged Device Model (FICDM) ESD testing is summarized in Table 3. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 3: ADSP-21479W-02 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	88-LFCSP	JS-002	1Ω, Cpkg	±1250V	NA	C3

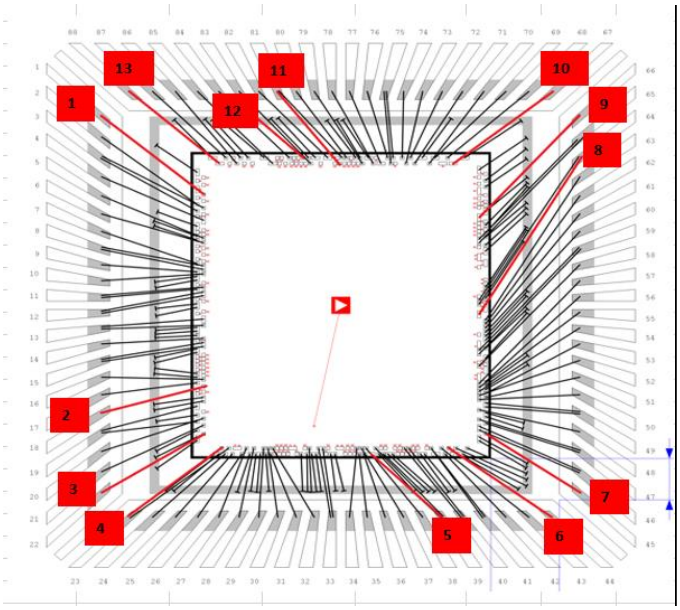
Approvals

Reliability Engineer: Jordan Placido

Additional Information

Data sheets and other additional information are available on Analog Devices' web site

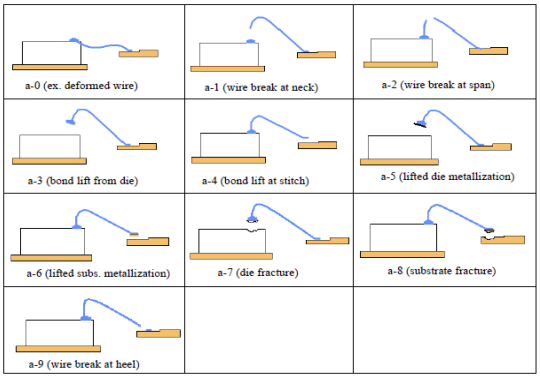
Appendix A: Post-TCT Wire Pull Test Results



Wire Pull Test Failure Modes

Mode	Description
a-0	Wire damaged/broken/missing prior test, or unsuitable for test
a-1	Wire break at neckdown point (reduction of cross section due to bonding process)
a-2	Wire break at point other than neckdown
a-3	Failure in bond (interface between wire and metallization) at die*
a-4	Failure in bond (interface between wire and metallization) at substrate, package post, or other than die
a-5	Lifted metallization from die*
a-6	Lifted metallization from substrate or package post
a-7	Fracture of die*
a-8	Fracture of substrate
a-9	Wire break at neckdown point on the substrate or package post

*For die-to-die wires, indicate the die of the break location (ex. D1, D2, etc.)



Unit	Q17607.1.TC1				Q17607.2.TC2				Q17607.3.TC3			
Ball	Force (gf)	Mode	Force (gf)	Mode	Force (gf)	Mode	Force (gf)	Mode	Force (gf)	Mode	Force (gf)	Mode
1	11.551	a-1	11.422	a-1	11.224	a-1	11.161	a-1	11.342	a-1	11.016	a-1
2	11.612	a-1	11.741	a-1	11.699	a-1	11.626	a-1	9.804	a-1	11.102	a-1
3	12.076	a-1	11.490	a-1	11.577	a-1	11.079	a-1	9.896	a-1	10.599	a-1
4	10.023	a-1	11.503	a-1	11.232	a-1	10.820	a-1	11.107	a-1	10.693	a-1
5	12.595	a-1	11.791	a-1	12.214	a-1	11.130	a-1	10.735	a-1	11.398	a-1
6	10.921	a-1	9.833	a-1	10.998	a-1	10.159	a-1	11.188	a-1	10.581	a-1
7	10.062	a-1	8.270	a-1	10.820	a-1	8.843	a-1	9.223	a-1	9.969	a-1
8	10.741	a-1	9.100	a-1	10.191	a-1	9.972	a-1	10.879	a-1	9.472	a-1
9	11.285	a-1	11.292	a-1	10.567	a-1	11.101	a-1	11.312	a-1	11.097	a-1
10	9.119	a-1	11.244	a-1	10.977	a-1	11.103	a-1	11.630	a-1	11.794	a-1
11	11.507	a-1	11.362	a-1	10.795	a-1	11.794	a-1	11.924	a-1	11.794	a-1
12	11.616	a-1	11.490	a-1	10.997	a-1	12.065	a-1	11.976	a-1	11.837	a-1
13	11.599	a-1	11.633	a-1	10.921	a-1	11.939	a-1	9.190	a-1	10.239	a-1
MIN	9.119		8.270		10.191		8.843		9.190		9.472	
MAX	12.595		11.791		12.214		12.065		11.976		11.837	
AVE	11.131		10.936		11.093		10.984		10.785		10.892	
STDEV	0.943		1.123		0.517		0.892		0.959		0.730	